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(54) Arrangement in data processing system for system initialization and reset.

(57) In computer systems deliberate initializations/resets of the processor latches which represent the internal processor states are necessary to erase only such information which is not required for a subsequent operation (e.g.processing/logging error data) prior to a processor start. One or more reset areas are defined which are initialized /reset in a staggered mode, where in each area a group of latches is assembled which have to be initialized/reset depending on the cause (e.g. power-on) for such a system initialization/reset. The latches within a reset area are connected to form shift registers which are initialized/reset by propagating a binary zero through all latches of the area(s) to be reset.

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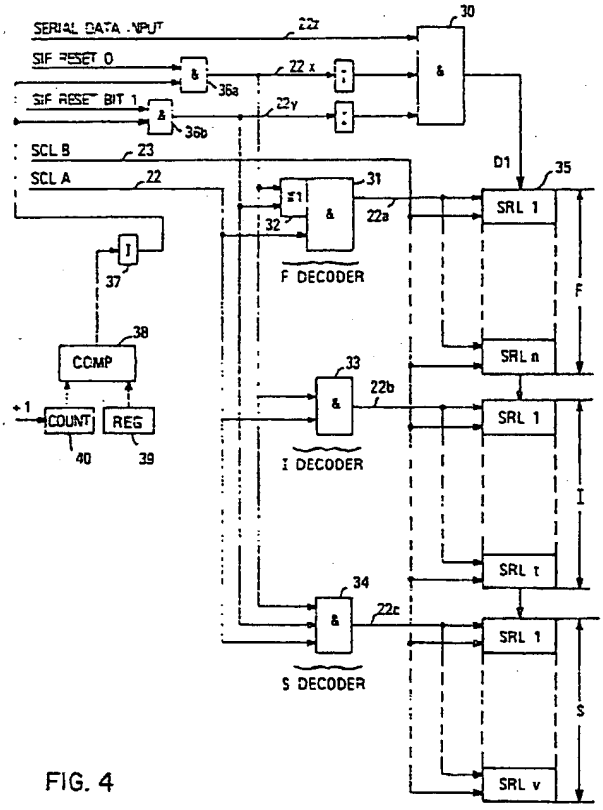
SERIAL DATA INPUT
22z
30
SIF RESET 0
36a
22x
SIF RESET BIT 1
36b
22y
SCL B
23
SCL A
22
D1
35
31
32
22a
F DECODER
37
38
COMP
+1
COUNT
REG
40
39
33
22b
I DECODER
34
22c
S DECODER
SRL 1
SRL n
SRL 1
SRL t
SRL 1
SRL v
F
I
S

FIG. 4

Arrangement in Data Processing System for System Initialization and Reset

The invention relates to an arrangement in a (self-guarding) data processing system for system initialization and reset.

In data processing systems deliberate system initializations and resets are necessary to erase or clear only such information which is not required for a subsequent operation, e.g. for logging or processing error data, for error correction, for repeating an interrupted operation in case of an intermittent error, or for maintenance.

In current data processing systems with dedicated service processors, system initializations and resets can be performed in partial areas of the central processing unit (CPU), depending upon a specific machine situation, (e.g. power on, failure, loading) by micro programs resident in a dedicated service processor via a respective service interface.

As already mentioned above, these selective and machine situation dependent initializations/resets are necessary to only clear or erase such information which is not required for a subsequent operation or which has to be in a known and definded initial state as a base for further processing.

In data processing systems without a dedicated service processor and systems, other than low cost systems where system initialization and reset is made by switching off and on the main switch, and causing a general reset, special measures have to be taken.

It is therefore an object of the invention to present a solution for selective (situation dependent) system initialization and reset actions within a data processing system.

Accordingly, an arrangement in a self-guarding data processing system is disclosed for system initialization and reset by setting the processor latches which represent the internal processor states to an initial state ("1" or "0"), which is characterized by a staggered initialization or resetting of the processor latches (SRL1...SRLv) arranged in reset areas (S,I,F), where in each area a group of latches is assembled which have to be intitialized/reset prior to a system restart, depending on the cause (e.g. power-on) for such a system intialization or reset, the reset areas being seriesconnected. Further features and advantageous embodiments can be seen from the subclaims.

The above described features result in the advantage of an effective handling of system initialization on reset in an electronic data processing system.

A complete understanding of the present invention may be obtained by refering to the accompanying drawings in which:

Fig. 1 is a schematic block diagram showing the general structure of a data processing system which forms the environment of the invention;

Fig. 2 is a block diagram of the reset structure;

Figs. 3 and 4 are block diagrams showing the circuitry necessary for system initialization and reset according to the invention, and

Fig. 5 is a pulse diagram of signals controlling the arrangements of Figs. 3 and 4 for performing system initialization and reset.

Referring now to Fig. 1, there is a block diagram of a conventional data processing system having various complex components which are interconnected by buses. As the figure shows, there is no dedicated service processor which can support a processing unit (PU) 1 for handling power on sequences, program loading, or error logging, analysis and recovery. A processor bus 10 connects the central control component, the processing unit 1, to a main memory (MM) 4 via a cache/main storage controller (cache CTL/ST-CTL) 3/5 and a main memory bus (MM-bus) 13. Processor bus 10 also connects the processor to an optional floating point processor 8 and at least to one I/O bus adapter 7. The I/O bus adapter connects processor bus 10 via an Input/Output bus (I/O bus) 9 to various Input/Output devices (I/O DEVs), and to further components such as communication adapters (COMM) etc. I/O bus adapter 7 is further designed to connect various control and monitoring components to the system, such as a customer engineering panel CE-P, a battery operated time of day clock TOD a read only memory unit ROM, an operator panel PAN, a power controller PWR-CTL or two supplementary devices SUPPL. A control store (CNTL-ST) 2 containing the control program is connected to the PU via a separate control store bus 11.

The system clock generation and distribution is centralized on a clock chip (CLCK) 6 which has multi-wire connections 14 to almost all of the system components. As an example, in the following description three initialization/reset areas are defined for processing unit 1. However, any other reasonable number of reset areas can be used. In the following reset concept which assumes three ranges of chained shift register latches (storage elements) which are used for implementing the system design in accordance with the level sensitive scan design rules (LSSD rules), the shift register latches are reset by flashing or ripple.

The level sensitive scan design rules are described in the article "A logic design structure for LSI testability" by E.B. Aichelberger, Proceedings of the Design Automation Conference No. 14, 20-22, June 1977, New Orleans, Louisiana, pp. 462-468.

The three reset areas are defined below:

- The S-area (power-on reset area) encloses all shift register latches (SRL) of the system, with the exception of those which are used to form storage arrays.
- The I-area (system reset area) includes all SRLs which are used as indication latches (check indicators). Latches, however, which are part of maintenance and/or service circuitry are not included. As an example, a microinstruction address compare register and the respective stop circuits of the PU chip 1 will not be reset. This offers the opportunity of checking and examining the system reset functions under conditions which are set into those registers.

The following listed functions which are manually invoked by the user force a system reset operation:
Initial Micro Code Loading (IML),
system Reset (with/without clearing the memory) and Loading Off the system program (with/without clearing the memory, IPL).

- The F-area assembles the function latches (check reset area). This area only includes the SRLs of the PU, which have to be reset into an error free state prior to restarting the PU for executing an error handling microprogram.

In order to avoid an uncontrolled processing or unscheduled behaviour of a PU, self-guarding actions based on check information contained in check circuits or checkers are never suppressed (no check stop override), which is the principle of an "always hot checkers" philosophy. By a selective reset of processor elements required for a new start of special microprograms, the error indicators and error stati which form "error images" survive the reset operation and can be accessed and processed by subsequent microprograms which are also guarded by the checking means.

The reset control (RS) 20 as shown in Fig. 3 is located on clock chip 6. Connected to the reset control 20 are all the reset request lines RRL, on which the signals can cause a total or partial system initialization or reset. The signals from top to bottom on the left side of Fig. 3 are the "power on reset" signal POR, the "initial micro program load" signal IML, the "system reset clear" signal SRC, the "system reset normal" signal SRN, the "load clear" signal LC and the "load normal" signal LN. These signals will be explained with more detail later on.

The reset operations as shown in Fig. 2 are system specific and based on hardware design and architectural requirements.

These reset operations can be arranged in a sequence according to the depth of their clearing effects on the hardware and logic areas within a data processing system. The most significant clearing action (power-on reset) can be considered as general actions supported by a sequence of single reset actions. The other reset actions involve less portions of the logic amount which means that more information is left in its original state.

The system reset clear signal SRC, the system reset normal signal SRN, the load clear signal LC and the load normal signal LN result in a reset of the latches of the I- and F-area.

A check reset CHR causes a reset of the latches of the F-area.

The given reset functions can alternatively be activated via a unit support interface (USI) for remote control purposes.

The reset control 20 has a set of output lines 21 to 24 for the transfer of various control signals to processor chip 1, floating point processor 8, storage controller 5 and to other chips which might be included in a computer system, an example of which is shown in Fig. 1.

Output line 21 is used to transfer the reset condition information, three bits in parallel, to the processor chip 1. Output lines 22 and 23 distribute the common clock signals, shift clock A (SCL A) and the shift clock B (SCL B), to the various chips. While shift clock A controls the master latches, shift clock B controls the slave latches of the chained shift register latches SRL.

The reset areas are further controlled by a two-wire line 24 which connects reset control 20 to the various chips with the exception of processor chip 1. The four different states of these two lines are sufficient to select the three given reset areas (S-, I-, F-; I - F; and F- only) and to indicate a "no-reset" state. Output line 21 consists of three wires thus being able to express 8 different states. These are the 7 different reset causes and one "no-reset" state. The 7 reset states are used in a twofold manner: 1) They designate the three reset areas and in addition to the two wire output line 24, they 2) provide the reset causes in detail. The reset causes are manifested in the so called reset indicator latches which can only be sensed (read) and reset by microinstructions of the error handling routines. The information which is stored in all those reset indicator latches allows a detailed analysis of the reason or cause of a system reset and

can be used later on for controlling the microprogram after restarting the computer system.

Output line 21 extends only to that chip which provides the logic required to access the reset information by microinstruction, which is the PU chip in this specific case.

Reset control 20 within clock chip 6 is further controlled by check reset signals which are activated by erroneous chips. The check reset signals are transmitted via so called stop lines 14 which are explained with more detail in European Patent Application 88 108 138.4.

T A B L E

KEY or SIGNAL	RESET COND. BIT: 0 1 2	SIF RESET BIT: 0 1	RESET AREA
Power on Reset	1 1 1	1 1	S, I, F
IML	1 1 0	1 0	I, F
System Reset Clear	1 0 1	1 0	
System Reset Normal	1 0 0	1 0	
Load Clear	0 1 1	1 0	
Load Normal	0 1 0	1 0	
Check Reset	0 0 1	0 1	F
NO Reset	0 0 0	0 0	-

The above table gives an survey with regard to the bit combinations forming the three-bit reset condition code which is transferred on line 21, the bit combinations of the two-bit area reset code transmitted on line 24, and the areas which are reset depending on the various input signals to reset control 20 fed on the RRL lines.

As shown in Fig. 4, the direct decoding of the signals on line 24 is used at the receiving side to connect the shift clock A (SCL A) to the master latches of the shift register latches SRL1 ... SRLn, SRL1 ... SRLt, SRL1 ... SRLv of the respective reset area F, I, S. Shift clock B (SCL B) is permanently connected to the slave latches of the shift register latches. The decoding of the SIF reset bits on line 24 is performed by the AND gates 31 - 34 and OR gate 32. When, for example, only reset area F has to be reset the SIF reset bit combination "01" has to be applied to line 24. The inverted bit combination on line 24 is also fed to AND gate 30, together with a serial data input. The output signal of AND gate 30 is, in any case a binary zero, with the exception of a code combination "00" which represents, however, a no reset condition, as can be seen in the table. With a binary zero at the input of SRL chain 35 and the pulses of shift clocks A and B, the binary zero is propagated through all stages of reset area F of shift register chain 35, thereby resetting all stages to zero.

A propagation beyond the F-area is not possible, because the coincidence condition for AND gate 31 is met only, and so shift clock A is transferred to the master latches of the F area only via line 22a.

When reset areas F and I are to be reset, e.g. in case of "load normal" (SIF reset code "10"), AND gate 33 will additionally be enabled so that the pulses of shift clock A will be transferred via line 22b to the master latches of the I-area. The binary zero already propagated through the F-area, continues through the I-area latches.

For "power-on reset" (SIF reset code "11") all three AND gates 31, 33 and 34 are activated so that shift

clock A pulses will be gated via lines 22a, 22b and 22c to all master latches of shift register chain 35.

Now the binary zero propagates through the register chain until its end.

The pulse diagram and the scheme of resetting the latches of shift register chain 35 which are represented in Fig. 5 show with more detail how the system is operated. The first two lines on top of Fig. 5 show the pulses of the shift clock A applied to the master latches, and of shift clock B for the slave latches of the shift register latches in shift register chain 35.

Line three shows a situation where a reset request, e.g. "system reset clear" (SRC) came in on line RRL. With the leading edge of the next shift clock A the reset indicator latches are turned on, as shown in line 4. The functional clocks which are also applied to the shift register latches and which are not shown will be stopped with the leading edge of the next shift clock B (line 5).

The reset condition code on line 21 and the SIF reset code on line 42 will be available with the leading edge of the next shift clock B (lines 6 and 7). After a natural delay caused by circuit delay the select signals for reset areas I and F are available, as shown in lines 8 and 9 of Fig. 5 as well as the forced zero at the input of shift register chain 35 (line 10).

Line 11 shows the pulses of gated shift clock A which is available on lines 22a and 22b.

The lower part of Fig. 5 shows the zero propagation through latches LT1 to LT2048 which form the shift register chain in this example. In each shift register stage the zero is transferred from its master latch M to its slave latch S. At the end of the propagation all latches or stages are reset to zero.

The maximum length of a reset chain in a given system determines the maximum count of counter 40 which is located in reset control 20. The counter is incremented in a close relationship to the shift clock pulses, and its count is transferred to a comparator 38. Register 39 is used to store a value which is equal to a preferred or selected number of shift register stages forming a chain, in the present example equal to the number 2048. Comparator 38 detects the situation when the actual count in counter 40 equals the preferred maximum length of the chain, the value of which is stored in register 39. In this case the output signal of comparator 38 changes from binary One to zero so that transmission gates 36 a and b do no longer transfer the SIF decode on lines 22x and 22y (decode 0 = no reset). This terminates the zero propagation.

If the maximum count would be smaller than the number of latches in the chain, the binary zero propagation would stop before reaching the end of the chain, leaving some latches in an undefinded state. Larger counts have no harmful influence because the zero propagation stops at the end of the chain.

Depending on the logic design of the processor circuitry the reset state for a certain individual latch within the chain must assume the opposite form, which means binary One. Those specific individual latches need an inverter stage at their input and their output (double inversion). Another more economic solution simply uses the "not Q" output of the preceding latch, and of the individual latch when the following shift register stage requires a zero reset state.

As further shown in Fig. 4, AND gate 30 generates the binary zero for propagation. Whenever the bits of the SIF reset code on line 24 differ from zero a binary zero is forced at the input D1 of chain 35 independent of what level is provided on the Serial Data Input line 22z which, in a non-reset state, provides the serial input data to the chain input D1.

Claims

1. Arrangement in a self-guarding data processing system for system initialization and reset by setting the processor latches which represent the internal processor states to an initial state ("1" or" 0"), characterized by a staggered initialization or resetting of the processor latches (SRL1...SRLv) arranged in individual reset areas (S,I,F), where in each area a group of latches is assembled which have to be intitialized/reset prior to a processor start, depending on the cause (e.g. power-on) for such a system intialization or reset, the reset areas being seriesconnected.

2. Arrangement as claimed in claim 1, characterized in that the processor latches of a reset area (group) (S,I,F,) are connected to form a shift register, the shift registers of the reset areas being chained together and controlled by a reset control (20) and logic gates (30 - 34) which, depending on the cause (reset request) generate control signals (reset condition bits, SIF reset bits, SCL A, SCL B) for resetting the processor latches of the F-area, the F-area plus the I-area, or the F-area plus the I-area plus the S-area by propagating a "0" through the latches of the F-area, of the F- and I-area, or the F-, I-, and S-area.

3. Arrangement as claimed in claim 1 and/or 2, characterized in that each individual shift register stage (e.g. SRL1) is composed of a master latch having a data input (D1) and an input (SCM1) for receiving a master shift clock (SCL A) and of a slave latch having a data input internally connected to the output of the

preceding master latch and an input for receiving a slave shift clock (SCL B), the output of the slave latch being connected to the data input of the succeeding master latch of the next shift register stage (e.g. SRL2) thus forming a shift register operated by applying the master shift clock via the logic gates (31 - 34) and by decoding the SIF reset bits for an area-selective resetting of the shift registers, the slave shift clock being directly applied.

4. Arrangement as claimed in any one or several of the preceding claims, characterized in that those shift register stages which require a "1" for initialization or reset have an inverter stage interconnected between themselves and their preceding shift register stages and themselves and their succeeding shift register stages.

5. Arrangement as claimed in any one or several of the preceding claims 1 to 3, characterized in that those shift register stages which require a "1" for initialization or reset have their master latch input connected to the inverse output (not Q) of the slave latch of the preceding shift register stage and their inverse slave latch output (not Q) connected to the input of the succeeding shift register stage.

6. Arrangement as claimed in any one or several of the preceding claims 1 to 5, characterized in that the maximum number of shift register stages accessed for initialzing/ resetting is determined by a predetermined count of a counter (40) which, when reached, switches an active reset pattern on the SIF Reset lines (22x, 22y) and the reset condition lines to an inactive state (no-reset image "00" or "000"), thereby determining the lengths of the zero propagation through one or more of the sequential reset areas (S,I,F).

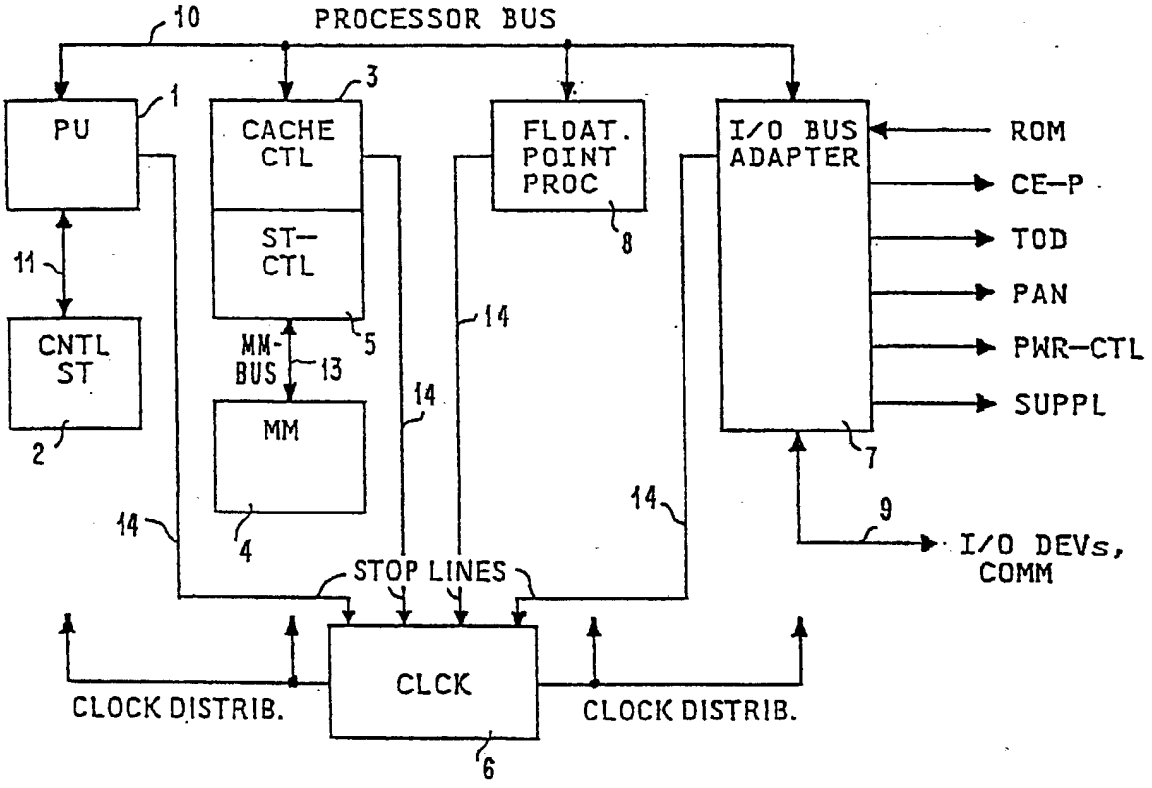
10
PROCESSOR BUS
PU
1
CACHE CTL
3
FLOAT. POINT PROC
8
I/O BUS ADAPTER
ROM
CE-P
TOD
PAN
PWR-CTL
SUPPL
ST-CTL
5
11
CNTL ST
2
MM-BUS
13
MM
4
14
14
14
7
9
I/O DEVs, COMM
STOP LINES
CLCK
6
CLOCK DISTRIB.
CLOCK DISTRIB.

FIG. 1

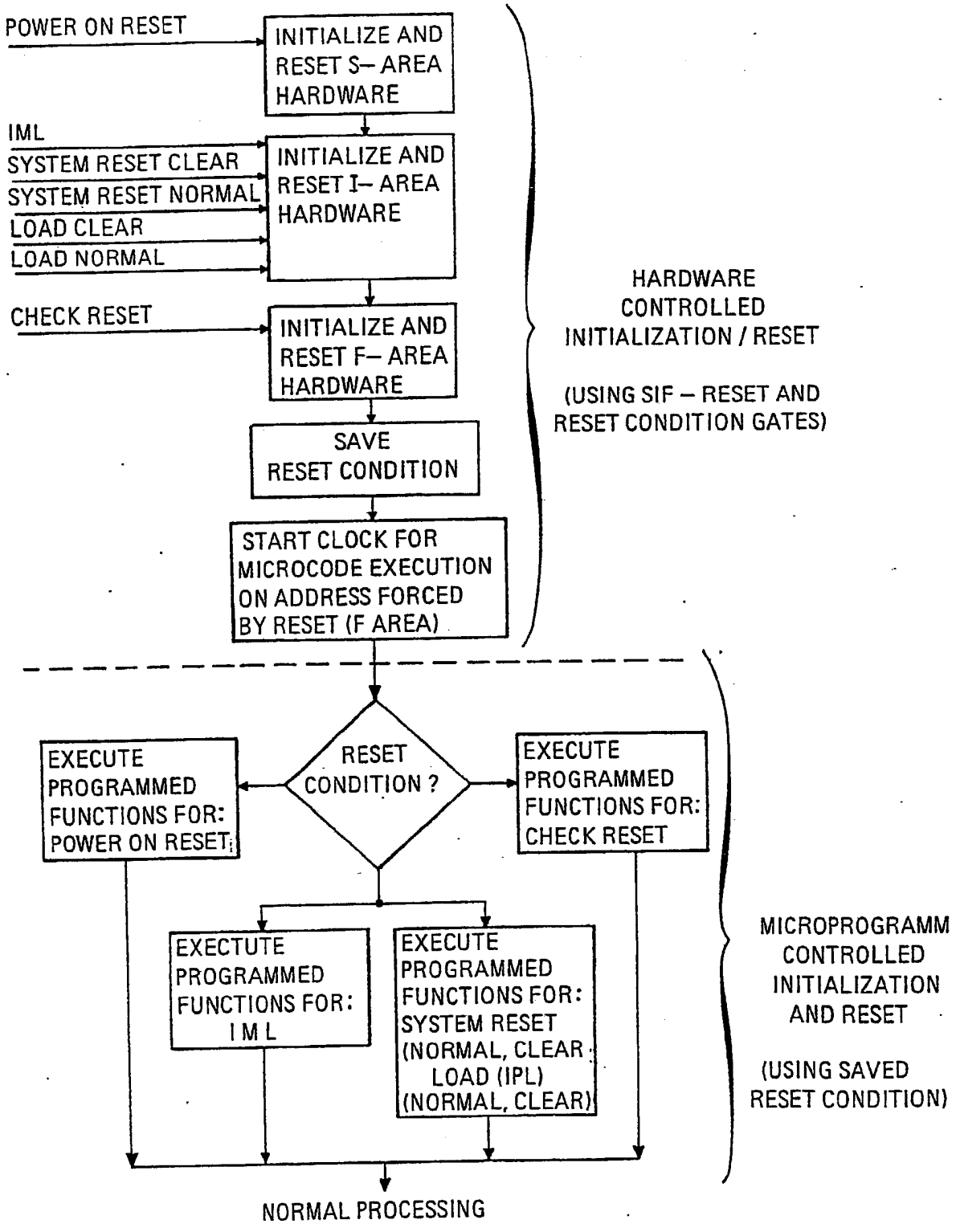
POWER ON RESET
INITIALIZE AND RESET S– AREA HARDWARE
IML
SYSTEM RESET CLEAR
SYSTEM RESET NORMAL
LOAD CLEAR
LOAD NORMAL
INITIALIZE AND RESET I– AREA HARDWARE
CHECK RESET
INITIALIZE AND RESET F– AREA HARDWARE
SAVE RESET CONDITION
START CLOCK FOR MICROCODE EXECUTION ON ADDRESS FORCED BY RESET (F AREA)
HARDWARE CONTROLLED INITIALIZATION / RESET
(USING SIF – RESET AND RESET CONDITION GATES)
RESET CONDITION ?
EXECUTE PROGRAMMED FUNCTIONS FOR: POWER ON RESET
EXECUTE PROGRAMMED FUNCTIONS FOR: CHECK RESET
EXECTUTE PROGRAMMED FUNCTIONS FOR: I M L
EXECUTE PROGRAMMED FUNCTIONS FOR: SYSTEM RESET (NORMAL, CLEAR LOAD (IPL) (NORMAL, CLEAR)
MICROPROGRAMM CONTROLLED INITIALIZATION AND RESET
(USING SAVED RESET CONDITION)
NORMAL PROCESSING

FIG. 2

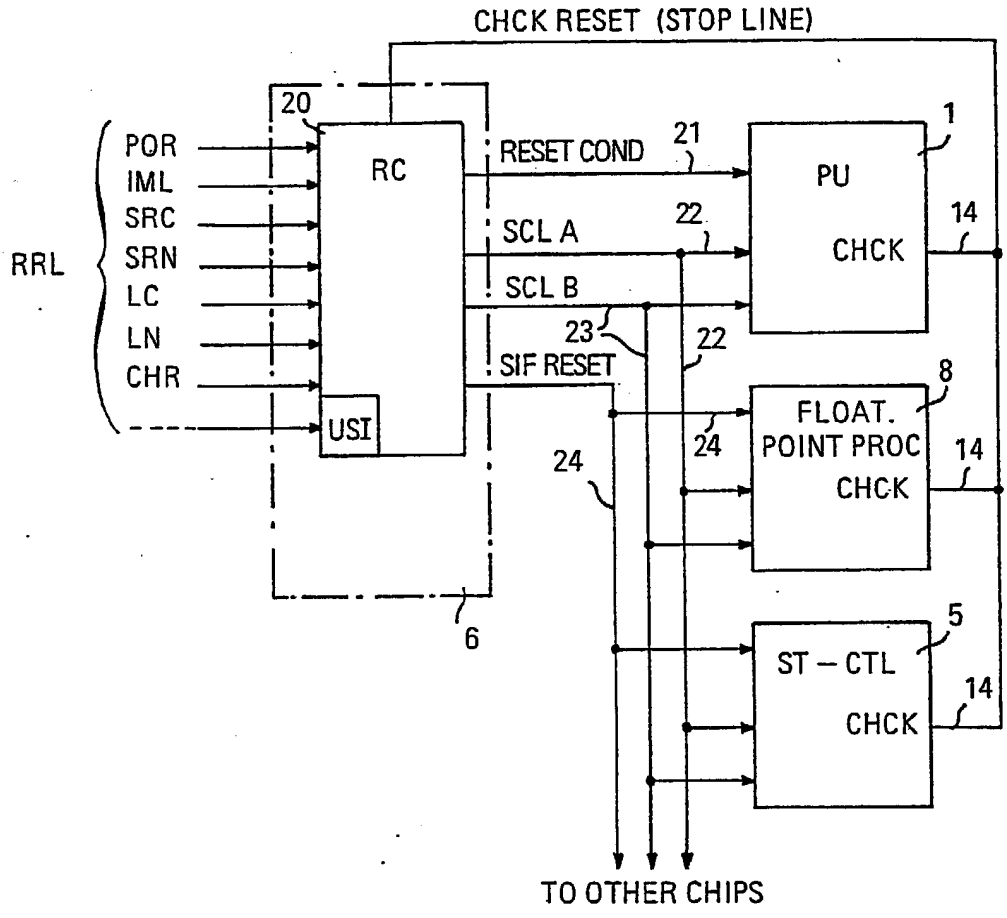
CHCK RESET (STOP LINE)
20
RRL
POR
IML
SRC
SRN
LC
LN
CHR
USI
RC
RESET COND
21
SCL A
22
SCL B
23
SIF RESET
22
24
24
6
PU
CHCK
1
14
FLOAT.
POINT PROC
CHCK
8
14
ST – CTL
CHCK
5
14
TO OTHER CHIPS

FIG. 3

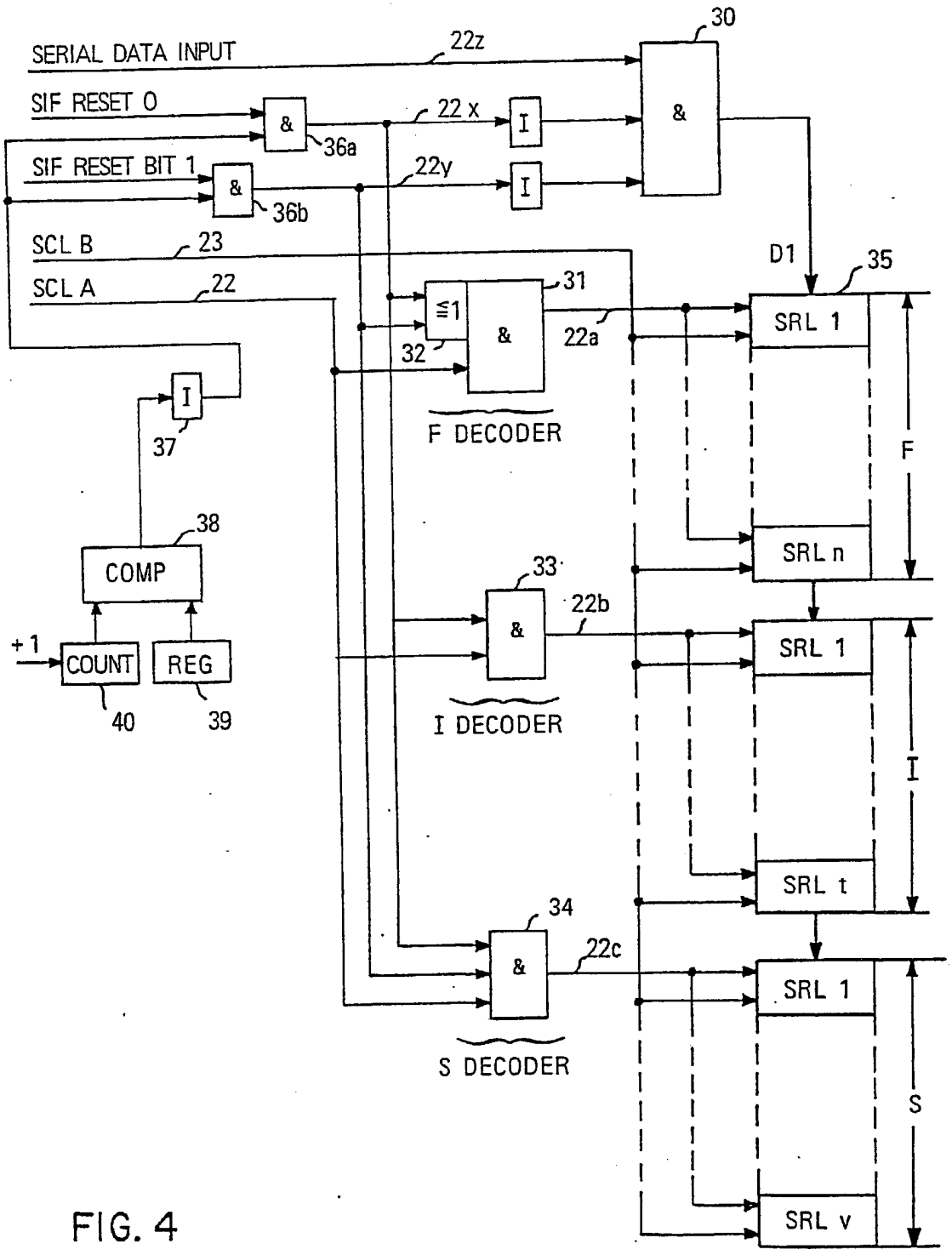
SERIAL DATA INPUT
22z
30
SIF RESET 0
&
36a
22 x
I
&
SIF RESET BIT 1
&
36b
22y
I
SCL B
23
D1
35
SCL A
22
≦1
&
31
22a
32
SRL 1
F DECODER
F
I
37
38
SRL n
COMP
33
22b
&
+1
COUNT
REG
SRL 1
I DECODER
40
39
SRL t
34
22c
&
SRL 1
S DECODER
S
SRL v

FIG. 4

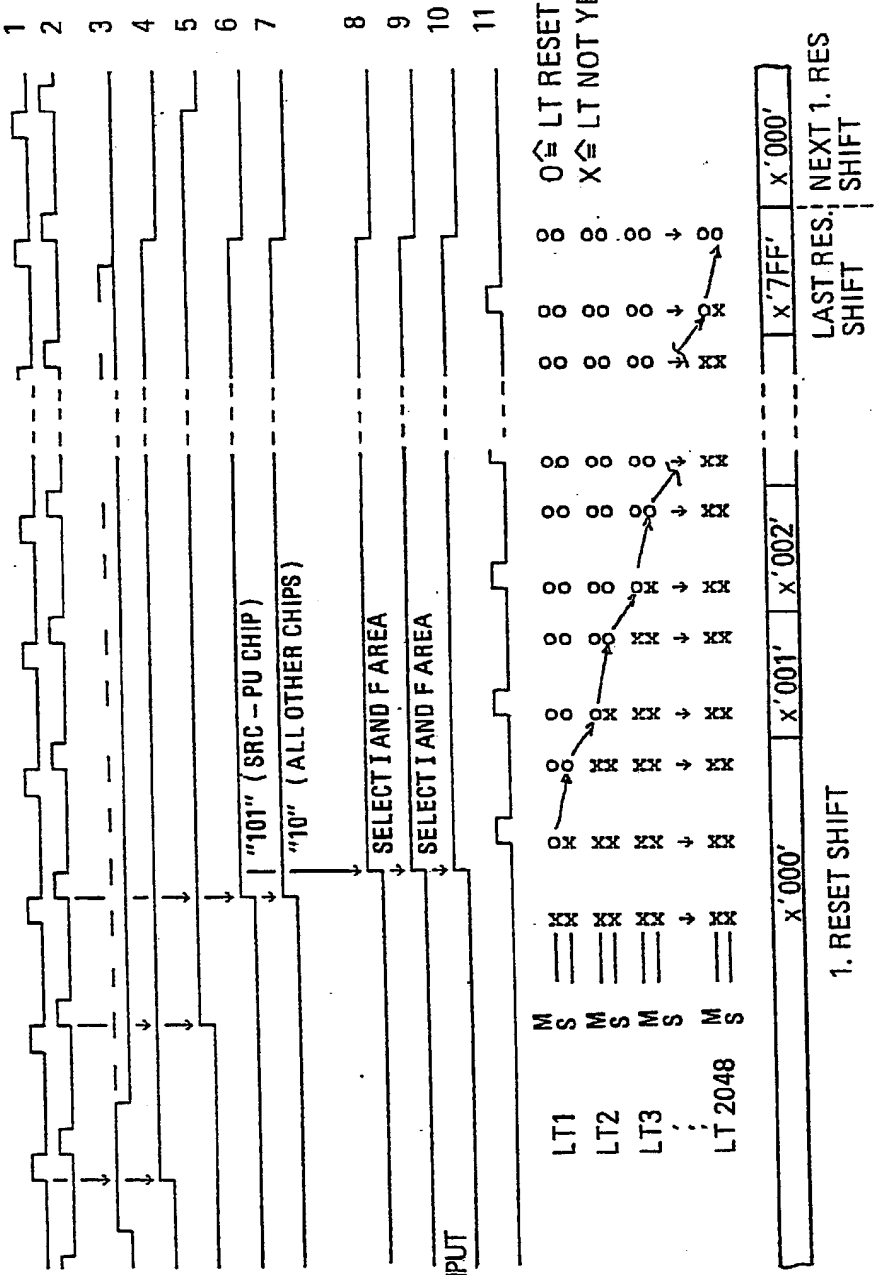
SCL A
SCL B
e. g. SRC ON RRL
RESET INDICATOR LATCHES
FCL STOPPED
RESET CONDITION ON 21
SIF RESET ON 24
DECODE SCR ACTIVE
DECODE SIF RESET ACTIVE
FORCED "0" AT CHAIN 35 INPUT
GATED SCLA
"101" (SRC – PU CHIP)
"10" (ALL OTHER CHIPS)
SELECT I AND F AREA
SELECT I AND F AREA
LT1
LT2
LT3
LT 2048
MS
RESET COUNTER
x'000'
x'001'
x'002'
x'7FF'
x'000'
LAST RES. SHIFT
NEXT 1. RES SHIFT
1. RESET SHIFT
0 ≙ LT RESET TO "0"
X ≙ LT NOT YET RESET
1
2
3
4
5
6
7
8
9
10
11

FIG. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 11 4023

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.3)
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 113 (P-276)(1550), 26th May 1984; JP - A - 59 020 025 (TOKYO SHIBAURA DENKI K.K.) 01-02-1984 * whole document *	1	G 06 F 1/00 G 06 F 11/00
A	IBM TECHNICAL DISCLOSURE BULLETIN vol. 28, no. 6, november 1985, page 2635, New York, US; "Hardware Reset of LSSD Logic Chip During System Operation (Fixed Reset)" * whole document *	1	
A	US-A-4 625 312 (BASHAW) * whole document *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.3)

G 06 F 1/00
G 06 F 11/00
G 06 F 11/26
G 06 F 9/44

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	03-04-1989	DURAND J.

CATEGORY OF CITED DOCUMENTS

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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)